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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/649,578

08/26/2003

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06/22/2006

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EXAMINER

FRANKLIN, RICHARD B

ART UNIT

PAPER NUMBER

2181

DATE MAILED: 06/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/649,578	Applicant(s) KIMURA ET AL.	
	Examiner Richard Franklin	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 9-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 11-13 is/are rejected.
- 7) ☐ Claim(s) 7, 9 and 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

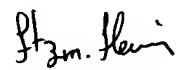
Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3/8/06.

- 4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____


FRITZ FLEMING
 PRIMARY EXAMINER
 GROUP 2100
 6/11/2006
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DETAILED ACTION

1. Claims 1 – 7 and 9 – 13 have been examined.

Drawings

2. The drawings were received on 22 May 2006. These drawings are acceptable.

Terminal Disclaimer

3. The terminal disclaimer filed on 22 May 2006 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on Application No. 10/649,228 has been reviewed and is accepted. The terminal disclaimer has been recorded.

4. Applicant's arguments filed 22 May 2006 have been fully considered but they are not persuasive.

Applicant argues that subject matter which was indicated as allowable in the previous office action has been added to independent claim 4, and since all claims depend from claim 4, all of the claims are allowable. The Examiner notes that the subject matter was indicated as allowable **only** if written in independent form including all limitations of the base claim and any intervening claims (emphasis added) (See Office Action Sent 22 February 2006; Paragraph 11). Also, the reasons for allowance state that the limitation is not taught **in combination with the other claimed elements** (emphasis added) (See Office Action Sent 22 February 2006; Paragraph 12). In the

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current amendment, Applicant has only added part of the subject matter from the objected to claims into the independent claim. This subject matter is not allowable by itself, and therefore, does not make claim 4 allowable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1 – 6, and 11 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lapstun et al. US Patent No. 6,687,022 (hereinafter Lapstun) in view of Applicants Admitted Prior Art (hereinafter AAPA) and further in view of US Patent No 6,665,088 (hereinafter Chiba).

As per claim 4, Lapstun teaches a data transferring apparatus for transferring liquid ejection data, comprising: a system bus (Lapstun; Figure 17 Item 145); an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development (Lapstun; Figure 17, Col 26 Lines 21 – 23); a receiving buffer unit comprising an interface memory for storing liquid ejection data compressed to be capable of line development (Lapstun; Figure 18 Item 146, Col 26 Lines 23 – 24); a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development and stored in the interface memory (Lapstun; Figure 17 Item 140, Col 28

Line 19 – Col 33 Line 41); a system memory for storing the liquid ejection data developed in the decode circuit (Lapstun; Figure 17 Item 82); a head controlling unit (Lapstun; Figure 17 Item 63); and wherein the interface unit, receiving buffer unit, the decode unit, and the system memory are coupled to the system bus in order to be able to transfer data (Lapstun; Figure 17).

Lapstun does not teach wherein the head controlling unit comprising a register of a liquid ejecting head.

However, AAPA teaches wherein the head controlling unit comprises a register of a liquid ejecting head (AAPA; Figure 15 Item 13, Page 2 Paragraph [0006]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Lapstun to include the register in the head controlling unit because this allows for the printhead to use data from the register and record an image (AAPA; Page 2 Paragraph [0006]).

Lapstun in combination with AAPA does not teach a first dedicated bus for coupling the interface unit to the receiving buffer unit; a second dedicated bus for coupling the receiving buffer unit to the decode unit; and a third dedicated bus for coupling the decode unit to the head controlling unit.

However, Chiba teaches a first dedicated bus for coupling the interface unit (Chiba; Figure 1 Item 11) to the receiving buffer unit (Chiba; Figure 1 Item 13); a second dedicated bus for coupling the receiving buffer unit (Chiba; Figure 1 Item 13) to the decode unit (Chiba; Figure 1 Item 15); and a third dedicated bus for coupling the

decode unit (Chiba; Figure 1 Item 15) to the head controlling unit (Chiba; Figure 1 Items 17 and 27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Lapstun in combination with AAPA to include the dedicated busses because doing so allows for faster communications between the different units.

As per claim 1, Lapstun also teaches a data transferring unit for transferring the liquid ejection data compressed to be capable of line development to the decode circuit via the system bus and transferring the developed liquid ejection data to the system bus (Lapstun; Col 27 Lines 62 – 64).

As per claims 2 and 5, Lapstun in combination with AAPA and Chiba also teaches a data transferring apparatus for transferring liquid ejection data including decode unit comprising a line buffer for storing the liquid ejection data developed by the decode circuit by word unit (Lapstun; Figures 29 and 30, Col 37 Lines 9 – 25); a transferring unit for performing transfers on the liquid ejection data compressed to be capable of line development to the decode circuit from the system memory (AAPA; Figure 15 Item A, Page 2 Paragraph [0006]), performing transfers on the liquid ejection data developed in the decode circuit to the system memory (AAPA; Figure 15 Item B, Page 2 Paragraph [0006]), and performing sequential transfers on the developed liquid ejection data stored in the system memory to a register of a liquid ejecting head (AAPA;

Figure 15 Item C, Page 2 Paragraph [0006]); and wherein the transfers are DMA transfers (Chiba; Col 5 Lines 65 – 67).

As per claims 3 and 6, Lapstun in combination with AAPA and Chiba also teaches wherein the line buffer further comprises two (2) faces of buffer areas for storing developed data and the liquid ejection data developed by the decode circuit is sequentially stored in the first face of the buffer, while the liquid ejection data developed by the decode circuit is sequentially stored in a second face of the buffer areas (Lapstun; Figures 29 and 30, Col 37 Lines 9 – 25); and transfers to the system memory is performed (AAPA; Figure 15 Item B, Page 2 Paragraph [0006]).

As per claim 11, Chiba also teaches wherein one (1) Application Specific Integrated Circuit (ASIC) comprises the interface unit, the receiving buffer unit, the decode unit, and the head controlling unit (Chiba; Col 5 Lines 44 – 46).

As per claim 12, Lapstun also teaches wherein the compressed liquid ejection data is run length compression data, and the decode circuit can perform hardware development on run length compression data (Lapstun; Figure 19 Items 157 and 158, Col 28 Lines 51 – 53).

As per claim 13, Lapstun also teaches a liquid ejecting apparatus comprising a data transfer apparatus (Lapstun; Figure 2 – 8, Col 4 Lines 25 – 35).

Allowable Subject Matter

6. Claims 7, and 9 – 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

7. Claims 7 and 9 are allowable because the prior art of record fails to teach or suggest alone or in combination wherein ***the receiving buffer unit further comprises a command storing register which is accessible from the system bus; a header analyzing unit for analyzing a header of the liquid ejection controlling data; a command separating unit for separating a command from the liquid ejection controlling data according to the analysis result of the header analyzing unit and storing the command into the command register; and a data transfer controlling unit for storing liquid ejection controlling data, from which the command is separated, into the interface memory*** (emphasis added), as required by dependent claim 7, ***in combination with the other claimed limitations and limitations inherited from parent claims*** (emphasis added). The references are silent on analyzing the header of incoming data and separating controlling data from data to be printed in the interface unit.

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8. Claim 10 is allowable because the prior art of record fails to teach or suggest alone or in combination wherein ***the receiving buffer comprises a data separating unit for separating the liquid ejection controlling data stored in the interface memory into a command and liquid ejection data compressed to be capable of line development, and wherein the command is processed by a microcontroller coupled to the system bus*** (emphasis added), as required by dependent claim 10, ***in combination with the other claimed limitations and limitations inherited from parent claims*** (emphasis added). The references are silent on separating controlling data from data to be printed in the interface unit.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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